Increasing the Usability of Semiconductor LCI

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The problem:

- In electronics LCA, ICs represent a substantial fraction of cradle-to-gate impacts
- Die size and technology are impact drivers for ICs
- Determining die size and technology can be slow or costly

The solution:

- Guidelines for estimating die size and technology generation from readily available information

Increasing IC LCI Usability

In electronics LCI, ICs represent a substantial fraction of cradle-to-gate impacts

Increasing IC LCI Usability

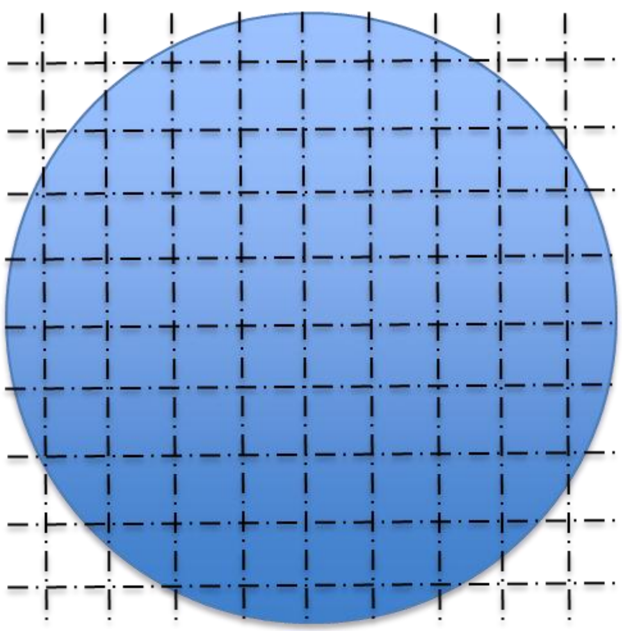
In electronics LCI, ICs represent a substantial fraction of cradle-to-gate impacts

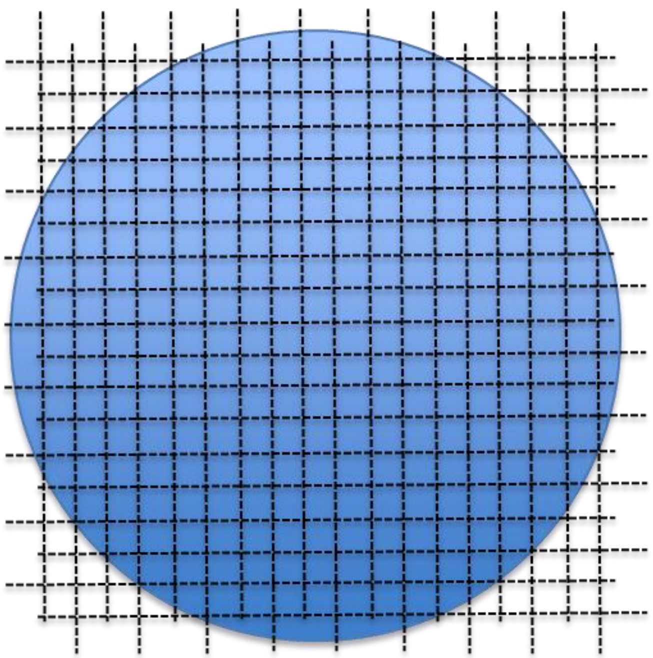
0.5 -30% of cradle-to-gate

Top GWP impact sources for ICs

- Use phase
- Energy use in wafer manufacturing
- PFC emissions in wafer fabrication
- Energy use in assembly and test

Importance of die size

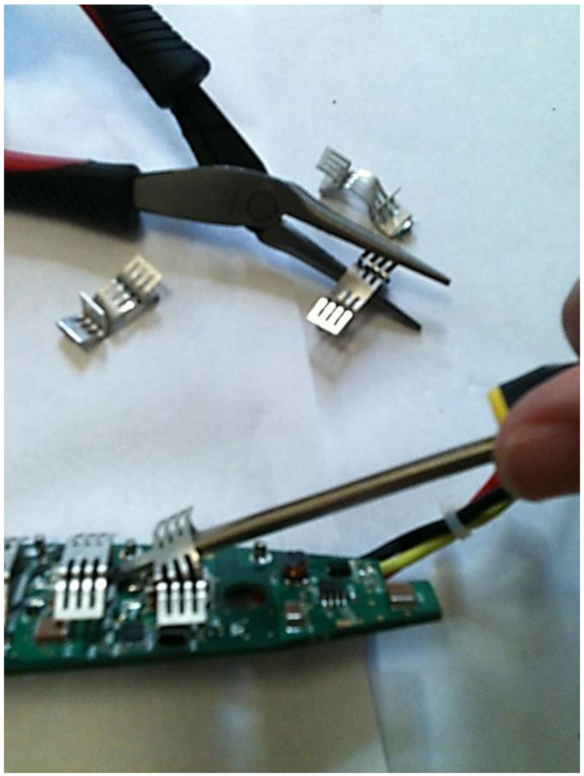


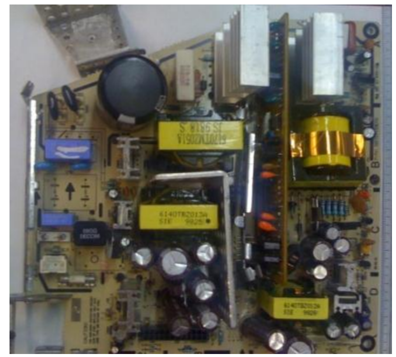


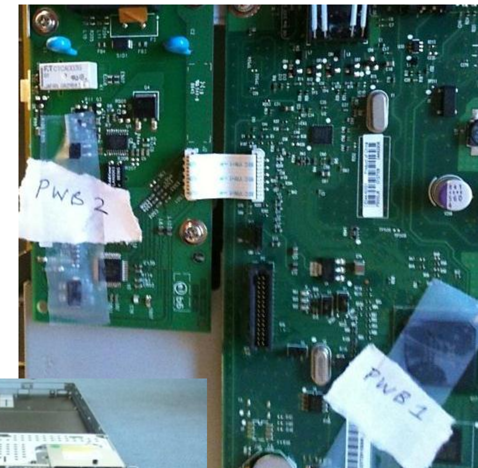
Strongly influenced by die area:

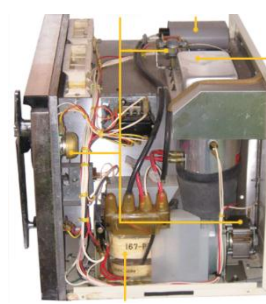
- Energy use in wafer manufacturing
- PFC emissions in wafer fabrication

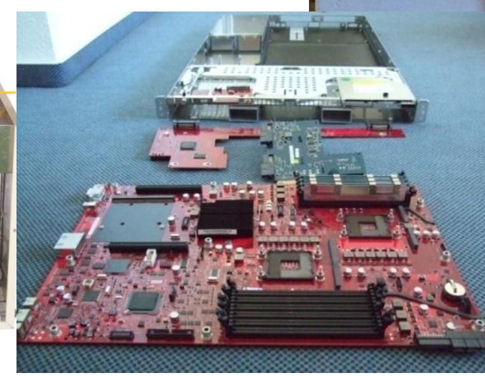
Even after all that disassembly







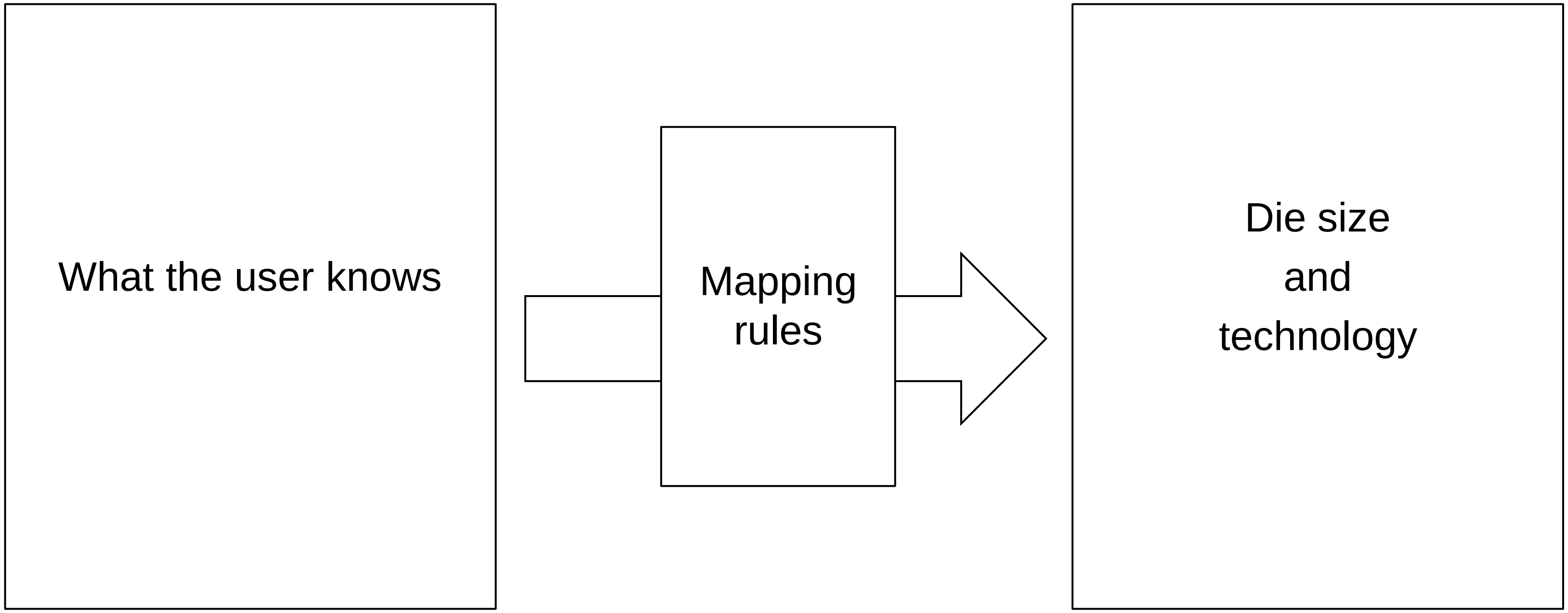




Determining die size and technology is slow or costly

- grinding
- x-ray imaging

Determining die size and technology for ICs



CPU

What the user knows:

Year of production
Model of processor
Package size
Number of cores
Graphics controller integrated?

Mapping rules

Critical parameters:

Technology generation
Die size

Determining die size and technology for a CPU

CPU

What the use

Year of production
Model of processor
Package size
Number of cores
Graphics controller

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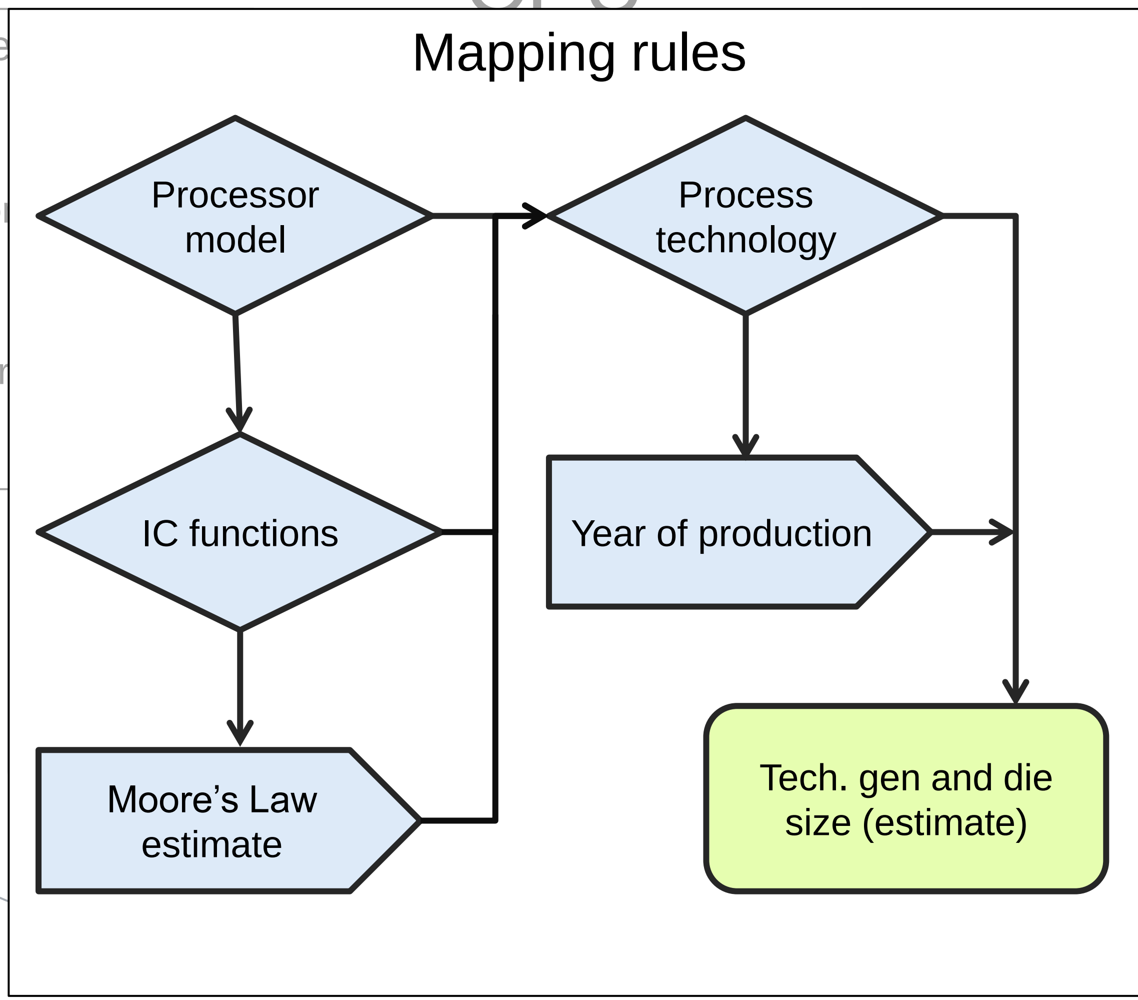
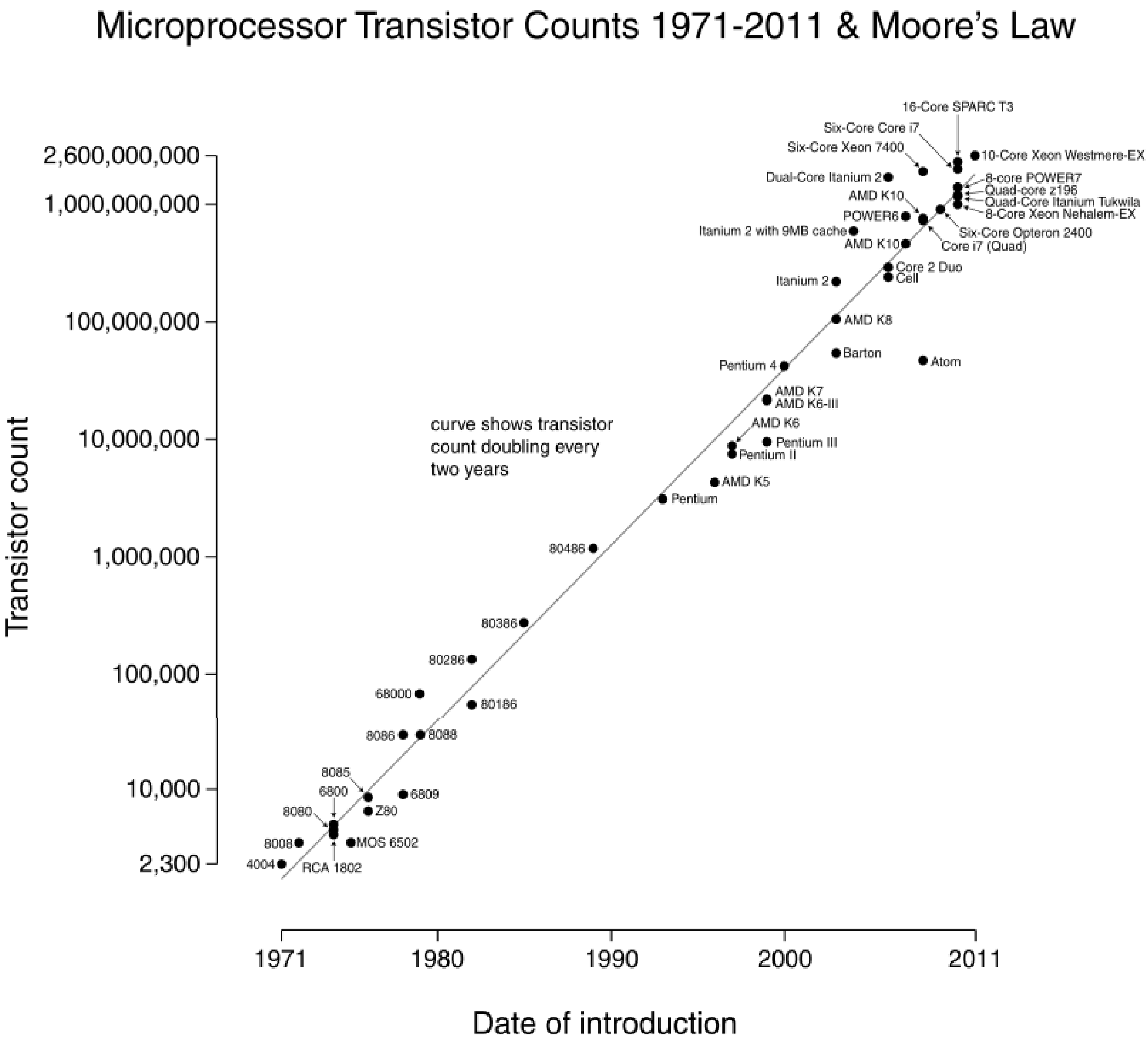


Moore’s Law and Transistor Counts



Estimating die sizes

A tool for roughly estimating die size:

Method 1:

$$\text{Die size (mm}^2\text{)} = \frac{\text{Known or functionality−informed CPU transistor count (M transistors)}}{\text{Expected transistor density: based on process technology (M trans./mm}^2\text{)}}$$

Method 2:

$$\text{Die size (mm}^2\text{)} = \frac{\text{CPU transistor count:estimate based on Moore's Law (M transistors)}}{\text{Expected transistor density: based on process technology (M trans./mm}^2\text{)}}$$

Expected transistor density for each process technology is reported and updated each year through the International Technology Roadmap for Semiconductors (ITRS)

Estimating die sizes

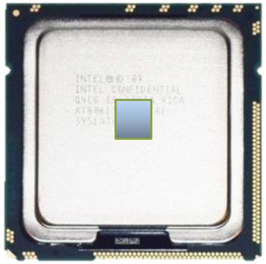
Example:

For mainstream production in 2013, 32nm process technology

$$\frac{1{,}000 \text{ Million transistors}}{700 \text{ Million transistors per cm}^2\ \dagger} = 1.4\ \text{cm}^2$$

Comparing with a hypothetical overestimate of 75% of package outer dimensions with

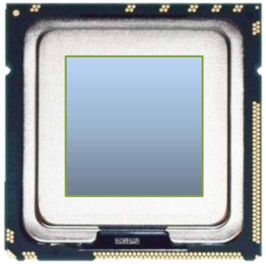
LGA 1366 package = 19 cm^2



1.4 cm^2 → 6 kg CO_2 eq

$$\frac{1.4\ \text{cm}^2}{19\ \text{cm}^2} = 7.5\%$$

6 kg CO_2 eq



19 cm^2 (75%) = 14 cm^2

14 cm^2 → 60 kg CO_2 eq

60 kg CO_2 eq

60 kg CO_2 eq

† 2010 ITRS: Cost performance MPU (Mtransistors/cm2 at production, including on-chip SRAM)

DRAM

What the user knows:

DRAM:
Memory capacity
Year of production
Number of chips

Mapping rules

Critical parameters:

Technology generation
Die size

DRAM

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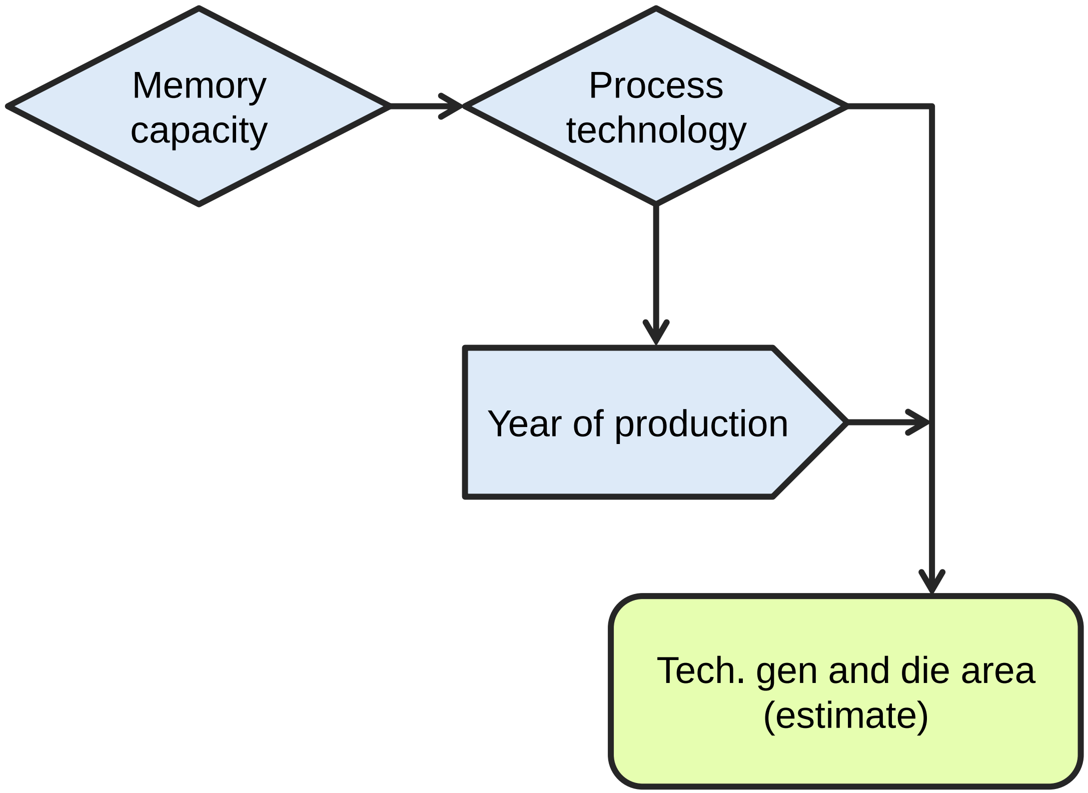
Mapping rules



Estimating die sizes

A tool for roughly estimating die size for memory:

$$\text{Die area (mm}^2\text{)} = \frac{\text{DRAM cell count: based memory capacity (GB)}}{\text{Expected cell density: based on process technology (M trans./mm}^2\text{)}}$$

Note: Flash memory is complicated due to multi-layer cells. 1, 2, or 4 GB capcity can be manufactured on the same die area, using the same process technology

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Thank you for your attention!

If you are interested in copies of the slides: s.boyd@pe-international.com